REMARKS

Claims 21-40, all the claims presently pending in this application, stand rejected upon informalities and on prior art grounds. Claims 21, 29, 35, and 38 are amended herein. In addition, the drawings and specification are objected to. The Applicant respectfully traverses the objections/rejections based on the following discussion.

I. The Objections to the Drawings

The drawings are objected to because the Office Action indicates that the drawings filed on April 8, 2004 are not readable. The Applicant traverses these objections for the following reasons. As indicated on page 13 of the amendment filed on April 8, 2004 (hereinafter, the "April 8th amendment"), a copy of the original application, as originally filed (together with the original informal drawings) were submitted with the April 8th amendment to illustrate that the Greek symbol μ given in the Applicant's original specification was incorrectly transformed into the notation Î¼ by the USPTO electronic filing process and/or software. Thus, the Applicant merely submitted a copy of the original specification and drawings with the April 8th amendment to illustrate that, as originally submitted, the application did not contain the above erroneous notation.

The drawings which accompanied the original specification were never meant to become replacement sheets for the previously submitted corrected formal (and clearly readable) drawings filed on October 17, 2003. In fact, the Applicant made no explicit or implicit request in the April 8th amendment to substitute the October 17, 2003 drawings with any other drawings, let alone with the drawings provided in the original application and submitted for the reasons outline

above. Therefore, the drawings filed on October 17, 2003 should constitute the current and pending drawings in the application, and as such, the Examiner is respectfully requested to withdraw his objection to the drawings for the reasons that they are not readable.

With regard to the objection that the connection in figures 3 and 5 are not complete, the Applicant notes that generally figures 3 and 4 of the Applicant's drawings show a functionally identical circuit. Likewise, figures 5 and 6 of the Applicant's drawings show a functionally identical circuit. The missing connections (i.e., dangling nets or stubs) in Applicant's figures 3 and 5 are merely provided to facilitate a better understanding of what circuit elements are removed during the migration of the circuit design from figure 2 to each of the respective situations (analog configuration of figures 3 and 4; and digital configuration of figures 5 and 6). Thus, the drawings as provided in the submission on October 17, 2003 greatly aids a reader's understanding and appreciation as to what is occurring in the progression of the circuit design to achieve the inventive results. As such, the Examiner is respectfully requested to withdraw his objection to the drawings for the reasons that the connection in figures 3 and 5 are not complete.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw all of the objections to the drawings.

II. The Objections to the Specification

The specification is objected to because the Office Action indicates that page 3, third paragraph (which is numbered as paragraph [0012]) is misleading. As such, paragraph [0012] has been amended in accordance with the Examiner's suggestion. More particularly, paragraph [0012] now reads, in part, "...wherein the rise in the input signal switches the tail current source

transistor off...." In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections to the specification.

III. The Claim Rejections

A. The 35 U.S.C. §112, Second Paragraph, Rejections

Claims 21-40 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These rejections are traversed as explained below.

Regarding claims 21 and 29, the Applicant has amended these claims to read, in part, "...whereby said rise in said input signal switches said tail current source transistor off..." in accordance with the Examiner's suggestion, thereby clarifying the claimed language. Furthermore, the Applicant has similarly amended claim 38 accordingly.

Regarding claim 25, the Office Action suggests that the claimed language is misdescriptive. However, the Applicant asserts that the claimed language directed to, "wherein as said input signal decreases, a switching threshold becomes dependent on said width-to-length ratio" is, in fact, correctly descriptive of the claimed invention. Specifically, the Applicant notes that the Office Action suggests that "[t]he increasing/decreasing of the input signal has no effect on a predetermined value W/L ratio of a transistor as recited [in the claims]." However, no such recitation is made in the claims, and in particular, claim 25. Rather, claim 25 indicates that as the input signal decreases, the switching threshold becomes dependent (is effected by) the width-to-length ratio. These are two separate concepts, and as such the Applicant suggests that the claimed language of claim 25 is correct and is not misdescriptive contrary to the assertion in the

Office Action.

Regarding claim 35, the Applicant has amended this claim to read, in part, "A comparator set to have a pair of trip points corresponding to a voltage value of a rising and falling edge of an input signal..." in accordance with the Examiner's implicit suggestions, thereby clarifying the claimed language.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw all of the rejections to the claims.

B. The Prior Art Rejections

Claims 21-40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kuo (U.S. Patent No. 5,483,184), in view of Lim, et al. (U.S. Patent No. 5,247,299), hereinafter "Lim". The Applicant respectfully traverses these rejections based on the following discussion.

However, as amended the newly added claims contain patentable features not taught in the prior art of record. Specifically, amended independent claims 1 and 29, recite in part, "...a plurality of transmission gates coupled to said transistors and adapted to select a reference signal and a comparator output signal for signal selection....". Additionally, amended independent claim 35 recites, in part, "...wherein said comparator cycles between an analog configuration and a digital configuration by selective selection of either said input signal or a ground signal through a plurality of transmission gates...."

The Applicant agrees with the Examiner that figure 3 of Lim shows transmission gates connected to the input transistors of the comparator to provide selective input signal selection. However, in Lim the two signals being selected are a reference signal (REF) or the power supply

voltage signal, V_{DD}, whereas in the Applicant's claimed invention, the two signals being selected include a reference signal (V_{REF}) or the comparator output signal (COMPOUT), not the power supply voltage signal V_{CC}.

Regarding figure 3 in Kuo, the tail current source transistor (M3) transitions between the analog and digital modes via direct control of the voltage level at the V_{in} pin. Conversely, in the Applicant's claimed invention, the transistor tail current source transistor (T1) transitions between the analog and digital modes through selective selection of either the COMPIN signal or the ground (GND) signal through two distinct transmission gates.

Furthermore, the additional features provided in the claims are simply not taught or suggested in the prior art of record, namely Kuo or Lim. Specifically, there is nothing to suggest that the prior art references teach that one of the trip points in their respective devices are provide external to the specific device provided.

Therefore, even if Kuo and Lim were combined in the manner suggested in the Office Action, they would still fail to teach all of the elements of the claimed invention. In fact, a combination of Kuo with Lim would tend to teach away from the claimed invention because column 4, lines 52-68 through column 5, lines 1-10 of Lim states that:

> The DAC output signal is coupled through a transmission gate 20 to the reference input of the comparator, i.e., the gate of M2. The function of the transmission gate 20 can be provided by any suitable circuit for selectively coupling the reference voltage from the DAC to the comparator input stage or conversely, decoupling the input stage, responsive to a control signal. In the preferred embodiment, a CMOS transmission gate is convenient. The new binary signal "sample/convert" is coupled to one of the control inputs of transmission gate 20. The sample/convert signal is coupled through an inverter 22 to the other transmission gate control input terminal.
>
> A transistor 24 is coupled between the comparator reference

input and the power supply rail VDD. Transistor 24 is controlled by the sample/convert circuit. In the preferred embodiment, transistor 24 is a PMOS device having its gate terminal coupled to the output of converter of 22.

In operation, when a voltage is being sampled, the sample/convert signal is high or logical "1", which couples the comparator reference node through transistor 24 to VDD. This has the effect of turning transistor M2 off, thereby setting the branch current I2 approximately to "0" and setting the branch current I1 equal to the comparator bias current Io. Transmission gate 20 is OFF.

Conversely, in the Applicant's claimed invention, as the COMPIN voltage continues to rise and becomes greater than the reference voltage at the V_{REF} pin, the voltage at node n4 sinks toward GND and the voltage at node n5 rises because the differential pair acts to allow less current to flow through T2 and more current to flow through T3. Less current flowing through T2 equates to less current flowing through T4 and less voltage being developed across T4 according to Ohm's law (V = I x R, where R is the resistance of transistor T4). The decrease in the voltage at node n4 causes inverter INV1 to switch and the voltage at node n1 to assume a logic high, which causes inverter INV2 to switch and the voltage at node n2 to assume a logic low. Similarly, the decrease in the voltage at node n4 causes inverter INV3 to switch and the voltage at node n3 to assume a logic high which causes inverter INV4 to switch and the voltage at node COMPOUT to assume a logic low.

This situation is shown in the HSPICE circuit simulation results of Figure 7 at time 5 µs, where the rising COMPIN voltage crosses the trip point voltage of 600 mV set by V_{REF}. This causes the COMPOUT voltage to fall to 0 V. In this state, the seven transmission gates of Figure 1 and Figure 2 change their state since the control voltages at nodes n1 and n2 have changed their

polarity. Thus, transmission gates, which were previously opened, are now closed and vice-versa. Thus, Lim teaches away from the Applicant's claimed invention, and even if Lim were combined with Kuo, it would still teach away from the Applicant's claimed invention.

Additionally, none of the prior art references of record, namely Kuo or Lim, describe the cycling timing of an analog versus digital configuration of a comparator, let alone that the digital configuration constitutes a majority of the cycle time. This unique feature allows the claimed invention to achieve greater power savings than the conventional devices.

In fact, Figure 7 of the present application shows two comparison cycles with each cycle approximately 31 μs in duration. In the first comparison cycle between times 0 μs and 31 μs, the inventive comparator is in the analog configuration between time 0 μs to 5 μs and time 30 μs to 31 μs for a total of 6 μs, and in the digital configuration between time 5 μs and 30 μs for a total of 25 μs. This clearly shows that the comparator is in the power saving digital mode for more than 80% of the comparison cycle time. Thus, because the claimed comparator dissipates less power than the devices provided in the prior art references, the claimed invention is much more ideal for use in low power applications than are the devices provided in the prior art references. The claimed invention is able to dissipate less power than the devices in the prior art references because the tail current is minimal when the invention's comparator is in the digital configuration, which, as provided by Figure 7, occurs during more than half of the comparison cycle time (i.e., a majority of the cycle time).

In view of the foregoing, the Applicants respectfully submit that the collective cited prior art do not teach or suggest the features defined by amended independent claims 21, 29 and 35 and as such, claims 21, 29, and 35 are patentable over Kuo and Lim alone or in combination with

one another. Further, dependent claims 22-28, 30-34, and 36-40 are similarly patentable over Kuo and Lim alone or in combination with one another, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define. Thus, the Applicants respectfully request that these rejections be reconsidered and withdrawn.

Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

V. Formal Matters and Conclusion

With respect to the objection/rejections to the specification and claims, the specification and claims have been amended, above, to overcome these objection/rejections. With respect to the objection to the drawings, the Applicant traverses these objections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections/rejections to the specification, claims, and drawings.

In view of the foregoing, the Applicant hereby submits that claims 21-40, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any

overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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Mohammad S. Rahman
Registration No. 43,029
McGinn & Gibb, P.L.L.C.
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (301) 261-8625
Fax: (301) 261-8825
Customer Number: 29154